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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,766	11/18/2002	Ting-Yu Chang	AOIP0005USA	9209

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
SELLERS, DANIEL R	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,766	CHANG, TING-YU	
	Examiner	Art Unit	
	Daniel R. Sellers	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see attachment*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

10/19/04
other 2 IDS's both dated 10/20/04 are duplicates

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 9, 11-17, and 20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Memran, U.S. Patent Application Publication 2002/0052665.

3. Regarding claim 1, see Memran

A computer system comprising:
a motherboard; and
an audio circuit integrated on the motherboard, the audio circuit comprising a Codec IC and a vacuum tube amplifier, wherein the Codec IC outputs an audio signal to the vacuum tube amplifier to amplify the audio signal. (p. 1, par. 0006 and par. 0007)

Memran teaches the use of vacuum tube circuitry in a computer system. It is inherent that a motherboard is used in a computer system and it is well known that motherboards may include integrated graphics, sound (i.e. a codec), networking, etc.

4. Regarding claim 2, the further limitation of claim 1, see Memran

... wherein the audio circuit further comprises an input end connected to the vacuum tube amplifier for inputting external audio signals, and an output end connected to the vacuum tube amplifier for outputting the amplified audio signal. (p. 1, par. 0008)

Memran teaches both an input end and an output end.

5. Regarding claim 3, the further limitation of claim 2, see the preceding argument with respect to claim 2. Memran teaches a resistor and capacitor connected to the tube (See also Fig. 1-4).

6. Regarding claim 4, the further limitation of claim 3, see Memran

... wherein the audio circuit further comprises a filament heating circuit for heating a filament of the vacuum tube to an operating temperature, and a voltage booster to provide the vacuum tube an operating voltage. (Fig. 1-4, unit 12 and heater element)

Memran teaches the use of a voltage booster and a heater circuit for proper operation of a vacuum tube.

7. Regarding claim 5, the further limitation of claim 2, see the preceding argument with respect to claim 1. Memran teaches the use of external signals and DVD players.

8. Regarding claim 6, the further limitation of claim 1, see the preceding argument with respect to claim 1. Memran teaches the use of vacuum tubes in computer audio circuits and the use of sound chips. It is well known in the art of computer electronics that a BIOS controls the functionality of computer peripherals, wherein the BIOS can selectively activate or deactivate certain functionalities. Therefore it is inherent that Memran teaches a switch for switching the integrated audio circuitry on or off.

9. Regarding claim 7, the further limitation of claim 1, see the preceding argument with respect to claim 1. Memran teaches that the Codec IC outputs audio, and it is inherent that it is output from a lineout port mounted on the motherboard (Fig. 3 and 4).

10. Regarding claim 9, the further limitation of claim 1, see the preceding argument with respect to claim 1. It is inherent that a computer system has a power supply for providing power to the motherboard.

11. Regarding claim 11, the further limitation of claim 1, see the preceding argument with respect to claim 1. Memran teaches the use of class-A amplification (see Fig. 1). It is inherent in the shown configuration that the vacuum tube is biased in class-A operation for linear amplification.

12. Regarding claim 12, the further limitation of claim 11, see Memran

... wherein the audio circuit further comprises a voltage amplifier for cascading with the class-A current preamplifier. (p. 2, par. 0021 and Fig. 4)

Memran teaches the use of cascading.

13. Regarding claim 13, the further limitation of claim 1, see Memran

... wherein the vacuum tube is a 9-pin double-triode vacuum tube. (pp. 1-2, par. 0017)

Memran teaches the use of 12AX7 vacuum tubes, which are a very common dual triode 9-pin vacuum tube used mostly in preamplifier circuits.

14. Regarding claim 14, see the preceding argument with respect to claims 1, 4, and 13. It is inherent that the vacuum tube is replaceable due to the fragile nature of vacuum tubes and their relatively short lifetime compared to solid-state devices.

15. Regarding claim 15, see the preceding argument with respect to claim 1 and 4. Memran teaches a method as such for amplification.

16. Regarding claim 16, the further limitation of claim 15, see the preceding argument with respect to claim 15. It is inherent that replacing resistors and capacitors change the amplifying characteristics of the circuit.

17. Regarding claim 17, the further limitation of claim 15, see the preceding argument with respect to claim 6. Memran inherently teaches a first switch.

18. Regarding claim 20, the further limitation of claim 15, see the preceding argument with respect to claim 4. Memran teaches the use of a heater circuit and a voltage booster for the proper operation of a vacuum tube.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Memran as applied to claims 1 and 15, respectively, above, and further in view of Palara et al., U.S. Patent No. 4,638,507 (hereinafter Palara).

21. Regarding claim 8, the further limitation of claim 1, see Palara

... further comprising a second switch connected to the audio circuit and a south-bridge chip for outputting a control signal to start up or shut down the audio circuit. (Col. 1, lines 29-59)

Memran teaches the use of vacuum tube technology with modern computers using solid-state technology. Memran inherently teaches a south-bridge, as it is well known in the art that motherboards have north and south-bridge chips for various control functions. Memran does not teach a second switch with these features. Palara teaches a switch for delayed turn-on of an amplifier circuit. It is well known that vacuum tubes need to reach operating temperature for proper linear amplification, and it would have been obvious for one of ordinary skill in the art to combine the teachings of Memran and

Palara for the purpose of delaying turn-on of the amplifier while the heating element brings the tube into proper operating bounds.

Regarding claim 18, the further limitation of claim 15, see the preceding argument with respect to claim 8. The combination of Memran and Palara teaches these features.

22. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Memran as applied to claims 1 and 15, respectively, above, and further in view of Hamano et al., U.S. Patent No. 6,347,035 (hereinafter Hamano).

23. Regarding claim 10, the further limitation of claim 1, see Hamano

... further comprising a frequency isolation wall for isolating the audio circuit from interference from other devices. (Col. 2, lines 20-30)

Memran teaches the use of vacuum tube technology with modern computers using solid-state technology. Memran does not teach a frequency isolation wall. Hamano teaches the use of an Electro-Magnetic Interference (EMI) shield to protect sensitive electronics from noise. It is well known in the art of amplifier design that EMI is most detrimental to the small signal stages (i.e. preamplifiers), and prudent design places the small signal stages away from digital clock signals and power supply circuitry. It is also well known that vacuum tubes are more susceptible to noise than the analogous solid-state components. It would have been obvious for one of ordinary skill in the art to combine the teachings of Memran and Hamano for the purpose of noise reduction.

Regarding claim 19, the further limitation of claim 15, see the preceding argument with respect to claim 10. The combination of Memran and Hamano teach these features.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sutherland, U.S. Patent Application Publication 2002/0198614 and the Asus P5-99VM SiS530 Socket 7 Motherboard webpage description as archived by the Web Archive (www.archive.org).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel R. Sellers whose telephone number is 571-272-7528. The examiner can normally be reached on Monday to Friday, 9am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SINH TRAN
SUPERVISORY PATENT EXAMINER

DRS